DEVELOPMENT OF FAST NbN RSFQ LOGIC GATES IN SIGMA-DELTA CONVERTERS FOR SPACE TELECOMMUNICATIONS

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ABSTRACT: *In the future generations of telecommunication satellites, it will be necessary to reduce the analog part in reception systems and to achieve RF front-end at higher carrier frequencies with higher sensitivity and higher bandwidth. RSFQ (Rapid Single Flux Quantum) superconducting logic is suitable to process very high speed digital data processing with very low power dissipation and with performances well beyond what should be possible with CMOS technology in the next decades. The RSFQ circuit technology based on superconducting niobium nitride (NbN) presently developed at CEA-G involves NbN/Ta_XN/NbN internally shunted Josephson junctions with high critical current density and high maximum switching frequency close to 1 THz, as required by ultra-fast RSFQ electronics. Very low power dissipation and very low noise level of fast NbN RSFQ gates designed and fabricated at CEA-G are presented. The RSFQ circuit for a sampling comparator has been studied operating in a sigma-delta modulator with a 30 GHz sinusoidal input carrier signal and a high sampling clock frequency of about 200 GHz. We will present the thermal noise and how it influences the phase fluctuations. Such a nitride technology has been recently demonstrated to be fully compatible with large scale integration on 200 mm diameter silicon wafer at reasonable fabrication cost in a micro-nano-electronic platform at CEA-Leti. The applicability of NbN RSFQ digital functions in the next decade Space Telecoms will finally be possible thanks to the development of reliable, low power consuming, space qualified cryocoolers operating at about 10K. Moreover semiconductor system design and integration techniques can be simply adapted to superconductivity, to fit the rules of any RSFQ library-foundry network, such as "CONNECT" for Japan and "FLUXONICS" for Europe.*

1 – INTRODUCTION TO RSFQ LOGICS

The need to increase traffic communications, i.e. the amount of information, requires a consequent increase in signal bandwidth and in carrier frequency. In the future generation of telecommunication satellites it will be necessary to reduce the analog part (LNA, RF filter, mixer, IF filter …) in reception systems to achieve a RF front-end at higher frequency with higher sensitivity, higher dynamics and increased range of linearity. The so called "Software Defined Radio" [1] reception systems will provide

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broadband applications, thanks to large bandwidth, high dynamic range Analog-to-Digital converter (ADC) devices, operating just behind the reception antenna and in front of digitally driven routers, packet switches, and high data processing throughput components.

In this context, the data processing rate and the sensitivity are the most significant parameters of any logic technology. However severe limitations will be observed at higher frequency operation, above 50 GHz, in the static and dynamic regimes of the semiconductor FET or HBT logic gates (based on Si, Si-Ge, AsGa or InP) due to strong increase in the local thermal dissipation with the frequency [2, 3, 4]. Such an increase in dissipation in fast logic functions will become overcritical especially for space telecom applications where both the electrical power supply and the possible thermal dissipation levels are limited at the satellite system level. As best example, the CMOS logic technology has to find radically new routes in order to achieve faster access times in the interconnections, a better thermodynamic gate efficiency with much lower static and dynamic dissipation levels, good impedance matching and accurate phasing at microwave frequencies. New solutions have also to merge in order to prevent cross-talk and punch-through between signal lines or between input and output of the gates as well to reduce leakage by tunnelling through very thin FET gate dielectrics (SiO_2 or high κ materials) [4, 5].

The application of RSFQ (Rapid Single Flux Quantum) superconducting logics [3, 6] should solve most of these forecasted semiconductor problems by taking large benefit from the natural features of superconductivity and of the Josephson effects. DC and AC Josephson fundamental phase relations [7, 8, 9] deliver very high accuracy only quantum limited, and high sensitivity up to THz frequencies [10, 11, 12]. At the same time superconducting stripe-lines and interconnections are not frequency dispersive and have very low noise and extremely low dissipation. For these reasons RSFQ technology allows reaching high speed digital processing with very low power dissipation. Superconducting devices [12] like clocks [13, 14, 15], flip-flops [13], 1024 bit shift registers [16], multiplexers (MUX) and demultiplexers (DEMUX) [17] and different analog-to-digital (ADC) architectures [18, 19, 20, 21, 22, 23, 24, 25] based on niobium (Nb) or niobium nitride (NbN) technology have been demonstrated to operate correctly at more than 40 GHz clock frequency at 4.2 K, opening new possible space based applications [10]. However the present RSFQ technologies require a shunt resistance in parallel with each Josephson junction to be damped. Such an externally connected resistance is the source of added parasitic elements, like inductances and capacitances, as well as impedance local discontinuities, causing an increase in the phase noise. Therefore this introduces a jitter in the clock generators and a consequent problem of synchronization at higher frequencies.

Research efforts have been recently devoted to study the self-shunted Josephson junctions such as Superconductor-Normal metal-Superconductor (SNS) or related junctions capable of producing high frequency Josephson currents with large enough amplitude [26]. The NbN technology developed at CEA involves NbN/Ta_XN/NbN internally shunted Josephson Junctions with high critical current density [27, 28, 29, 30] and high maximum switching frequency close to 1 THz.

We will present the principles of RSFQ logics based on NbN logic gates and their application to a sigma-delta modulator designed for a 30 GHz input signal carrier frequency, including a sampling clock operating at about 200 GHz. We will try then to

analyse the thermal noise in a SNS Josephson junction, showing how it causes the phase fluctuations and therefore a clock jitter.

We finally put emphasis on various fabrication aspects of NbN multilayer circuit technology based on a reliable process developed at CEA-G. By using an adapted RSFQ-"Fluxonics" library [31] and conventional packaging techniques, we present how NbN RSFQ should make feasible digital module operation for space telecom at about 100 GHz clock frequency and 10 K, temperature compatible with recently developed compact cryo-coolers [32].

2 – INTEREST IN NbN/Ta_XN/NbN JOSEPHSON JUNCTION FOR RSFQ GATES

Two superconductors separated by either a normal or a tunnel barrier form a Josephson junction, in which the current of charges (Cooper pairs) can cross the barrier without any voltage at the junction bounds below a critical value, I_C, following these two Josephson phase relations [7, 8, 9]:

$$I_S = I_C \sin\phi \tag{1}$$

$$V = \frac{2\pi}{\Phi_0}\frac{d\phi}{dt} \tag{2}$$

It is observed experimentally that for an applied bias current higher than the critical DC Josephson current, the voltage appearing across the junction is due to a combination of DC and AC flow of both Cooper pairs and "quasi-particles". The result is a partially resistive dissipation as well as both inductive and capacitive effects between the two electrodes sandwiching the barrier.

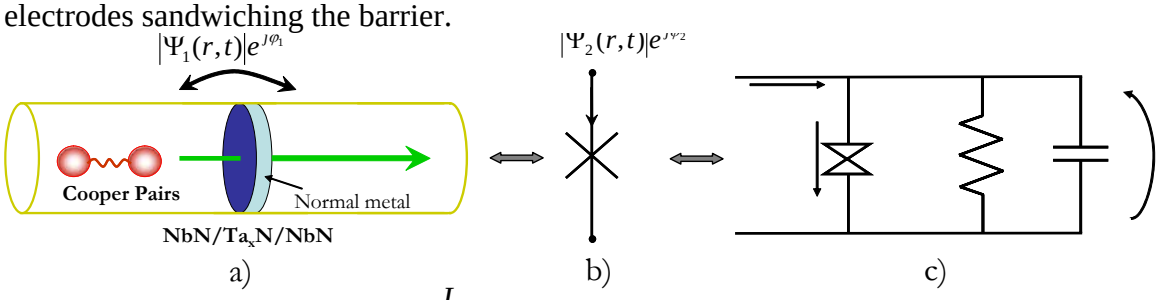

Figure 1 – Josephson junction. a) Physical principle applied to NbN superconducting electrodes and to a Ta_XN barrier. b) Circuital symbol. c) RCSJ (Resistively and Capacitively Shunted Junction) model.

A common model of the junction is shown in figure 1, and yields to the following normalized time equation of Josephson phase, where $i = I / I_C$ is the normalized current:

$$i = \beta_c \ddot{\phi} + \dot{\phi} + \sin\phi \tag{3}$$

in which it appears a typical damping parameter called the McCumber-Stewart factor:

$$\beta_c = \frac{2\pi R I_C}{\Phi_0} RC \tag{4}$$

Depending on its value, we can obtain an internal shunted junction ($\beta_c \leq 1$) or a hysteretic junction ($\beta_c > 1$). Equation (4) depends on the capacitance *C* and on the *RIc* product. When internally defined into the junction planar area, these parameters do not

depend on the surface of each junction achieved on a specific chip. They are rather related to the specific barrier properties: insulating barriers are controlled by thickness, dielectric permittivity and tunnel transparency and normal metal (N) or related barriers are determined by diffusive or ballistic parameters in a coherent transport of Cooper pairs [26].

If we consider a SNS junction the capacitance is very small and it is easy to achieve $\beta_c \leq 1$ and a current-voltage characteristic like figure 2.a. The shown voltage is the time averaged of the $V(t)$ corresponding at the solution of the differential equation for different bias current values. We can see in the figure 2 two different states, a superconducting state for $I < I_c$ and a resistive state for $I > I_c$. If we bias the junction at a fixed current value above the critical current, we will observe a periodic 2π phase shift corresponding to a voltage pulse emitted across the junction at the Josephson frequency of equation (2). In a similar manner if we send a simple current pulse across the junction (or a single voltage pulse through an inductance coupled to the junction), this pulse will be added to the DC bias current, and exciding the junction critical current, and inducing a single voltage pulse at the junction output.

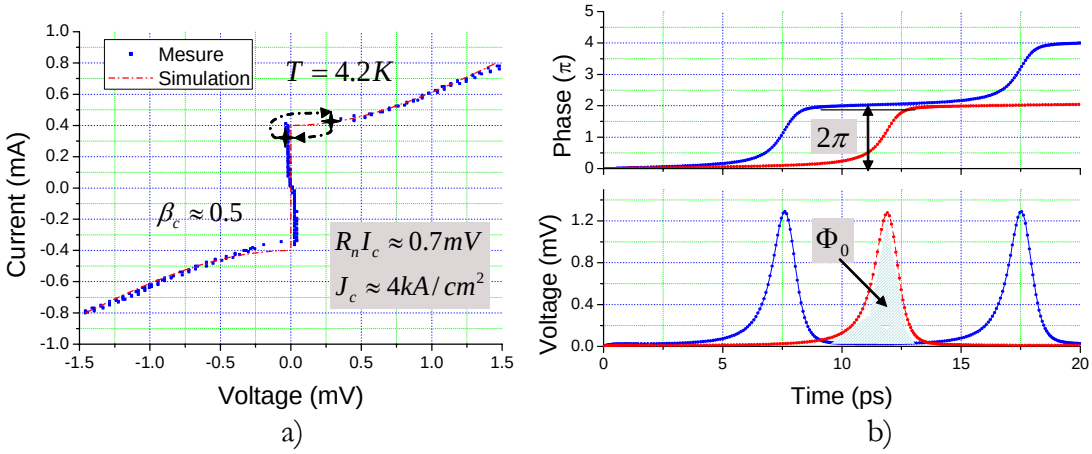

Figure 2 – a) Experimental I-V characteristics of a 4 µm diameter NbN/Ta_XN/NbN Josephson junction measured at 4.2K [10]. b) Simulation of the time dependence of Josephson phase and of junction voltage; each time the total current crossing the junction exceeds the critical current a 2π phase shift is observed, and a voltage pulse appears across the junction; a logic bit "1" is generated when a single pulse appears between two clock pulses at the Josephson frequency.

Each of these pulses has a quantified "*voltage* x *duration*" area equal to a single flux quantum, $\Phi_0 = h/2e \approx 2.07mV.ps$, and they transport the information in the RSFQ logic as shown in figure 2.b. If a voltage pulse appears between two clock pulses generated at the Josephson frequency by a closely similar junction inside the logic gate, the logic bit "1" is obtained, "0" in other case.

The time width of each single pulse is given by the following relation:

$$\tau_W = \frac{\Phi_0}{2\pi R_N I_C} \tag{4}$$

To achieve high frequency operation the pulse must at least be five times smaller than a clock period. Consequently in order to get fast RSFQ logics, one needs high $R_N I_C$ product

in the junction which is difficult to achieve with most of the SNS junctions [26]. SNS junctions are often overdamped by a low resistance barrier layer and very sensitive to decoherent factors such as finite temperature and barrier material heterogeneities [10]. Ta_XN barriers close to the insulator-metal transition offer an attractive alternative to classical SNS with normal or superconducting metal barriers [26]. As well, the relatively high critical temperature of NbN superconductor films (up to 16.5 K) offers a larger domain of operating temperatures (from 4 K to 12 K) than niobium based circuits, limited to 4 K.

In our experiment we measured a Josephson junction with a $R_N I_C$ of 0.7 mV, therefore capable to produce short pulses of 0.5 ps duration with an extremely low dissipation level:

$$\Delta E = \int IVdt = \frac{\Phi_0}{2\pi}\int Id\phi \approx \frac{\Phi_0}{2\pi} I_C 2\pi = I_C \Phi_0 \approx 10^{-20} J \tag{5}$$

for each logic pulse.

The interest in the RSFQ logic devices is the very low static and dynamic gate dissipation allowing pulsed logics to be much more thermodynamic efficient than hold and latch FET logics. Moreover RSFQ gates are not far from ultimate reversible logic gates such as involved in “Quantum-bits”, for instance they have been recently applied to fast read-out of phase and flux “Qu-bit” gates.

3 – NbN FAST SIGMA-DELTA MODULATOR COMPONENTS

In order to apply this RSFQ technology to ADC Sigma-Delta architecture for a SDR system, we studied the two principle gates, the clock and the comparator or one-bit quantifier, needed for a 30 GHz input signal carrier frequency and a sampling frequency of 200 GHz. We will show in this section the design and the simulation of these gates, explaining the behaviour of a Josephson Transmission Line (JTL) and its application in the RSFQ logics.

3.1 – CLOCK

The most simple clock design is a Josephson junction biased with a current over its critical current value to obtain the so called *AC effect*. The junction is switching at the Josephson frequency (~ 483 GHz/mV) between the superconducting state and the resistive state:

$$f_J = \frac{\overline{V}}{\Phi_0} \tag{6}$$

where $\overline{V}$ is the mean voltage over a period. If for instance we polarize the $NbN/Ta_XN/NbN$ Josephson junction measured in figure 1.a with a current ratio $I / I_c \approx 1.1$, we obtain a mean voltage corresponding in figure 1.a to 0.414 mV which gives, from the equation (5), a frequency of about 200 GHz. We will employ this clock generator for our Sigma-Delta modulator and we will add a JTL to improve the oscillations quality, as shown in figure 3. JTLs transmit the input signal to the output and can amplify input pulses with an increase in the Josephson junction critical current. The Josephson junctions employed in the JTL circuit have the same critical current density, while the last junction, J_4, is bigger and the clock oscillations are amplified.

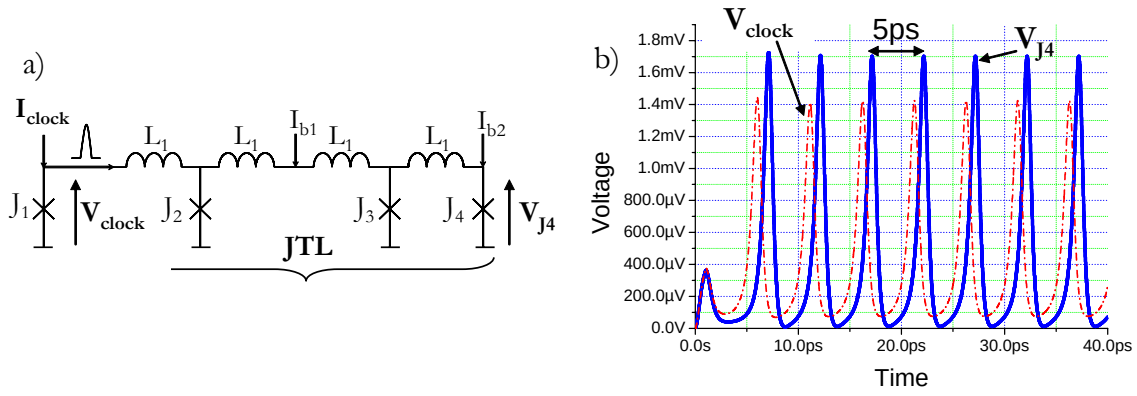

Figure 3 – a) Clock circuit design with a Josephson transmission line. b) Simulation result with JSIM [33]. The greater signal is the output of the JTL following the JTL amplification.

3.2 – COMPARATOR

The comparator or one-bit quantifier is the decision element in a sigma-delta modulator. It samples the input signal at the clock frequency producing at its output a logic number either "1" or "0" depending on its threshold level. Normally this level is fixed in order to obtain 50% of "1" and 50% of "0".

In the RSFQ logics the comparator is based on two identical Josephson junctions [34, 35] as shown on the figure 5.a. The input signal is injected at the born of the junction

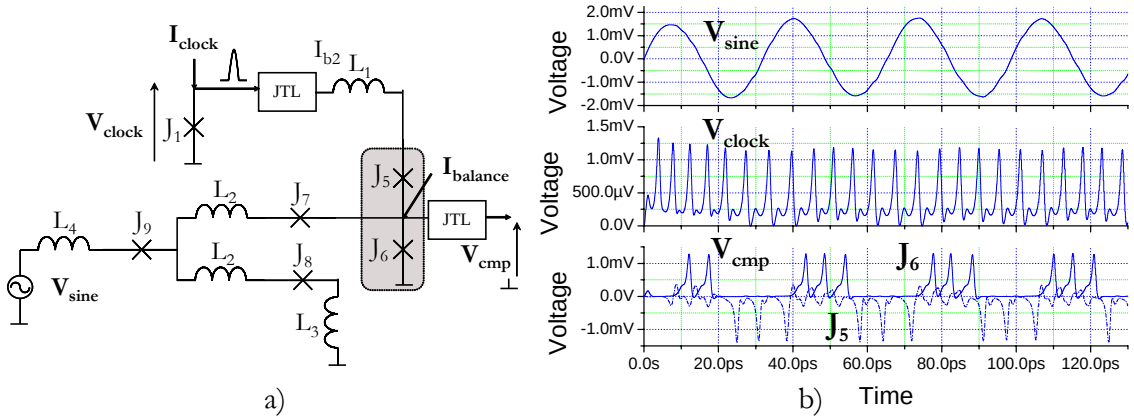

Figure 4 – a) Comparator circuit design with a Josephson clock sampling rate of 180 GHz and a 30 GHz input sine. b) Simulation result with JSIM [33] of (from top to bottom) input signal, clock and comparator junctions. The output of the comparator $\mathbf{V_{cmp}}$ is taken over the J_6 junction.

J_6 with a SQUID (Superconducting QUantum Interferometer Device) formed by L_2, L_2 and L_3 inductances and J_7 and J_8 junctions. The sinusoidal current is added to the clock current coming across the junction J_5. Josephson junctions are chosen in order to avoid non desired switching. In this circuit design we have a 0.51 mA critical current for the comparator junctions, 0.48 mA for the SQUID junctions, and 0.54 mA for the junction J_4 of the JTL shown in the figure 3.a. We added another bias current over the J_6 junction for

adjusting the balance of the comparator. In practice the two junctions in the comparator are showing the same behaviour as a normal balance. Junctions switch alternatively depending on the current crossing each junction. When J_6 is in the resistive state, J_5 is in the superconducting state and vice versa. The $I_{balance}$ bias current allows choosing how long the junction J_6 should keep this state. In other terms, with $I_{balance}$ we can control the number of logic 1 at the born of the J_6 junction. Figure 4.b shows a simulation of the comparator operating with a 30 GHz sinusoidal input signal and with a clock frequency of 180 GHz. The total current crossing the J_6 junction is the sum of the clock current and the sinusoidal input current. When this value exceeds the J_6 critical current, a voltage pulse at the output is generated behind the JTL. Figure 4.a shows the output of the comparator with a balance current of 0.35 mA corresponding to a threshold of 0 V for the input sine. Consequently the number of voltage-state is the same for J_5 and J_6 junctions, that is three logic "1" bits and three logic "0" bits.

In this simulation we have adjusted the bias current of the clock at a value larger than the case of figure 3, for a current ratio of 1.35, because of the influence of the other circuits like the SQUID and the comparator. If we increase the current ratio of the clock junction we must adjust the $I_{balance}$ current to obtain the same behaviour. We have then increased the clock bias current to reach the 200 GHz desired for our sigma-delta modulator, but we couldn't distinguish the output pulse in phase between two clock pulses, to determine whether it was a logic "1" or logic "0". As 180 GHz is a multiple of 30 GHz, synchronization is achieved, so with this operation condition, we can locate each pulse in a clock period.

3.3 – NOISE SOURCES IN CIRCUIT OPERATION

RSFQ circuits are not immune to noise sources. One of the typical influences is due to the thermal noise, or Johnson-Nyquist noise, of the R_N normal resistance. The spectrum is well known as:

$$S_I = \frac{4k_B T}{R_N} \tag{7}$$

As a Gaussian white noise we can model this noise as a random current in parallel with the Josephson junction and with a root mean square given by the Nyquist Formula:

$$i_{rms} = \sqrt{\frac{4k_B T f_c}{R_N}} \tag{8}$$

For a 10 K operation and a bandwidth of 200 GHz, we found a 7 μA noise current root mean square, which is the 1.3% of the Josephson mean critical current value.
This random signal must be considered in equation (3) as an additional current noise $i_N(\tau)$:

$$\beta_c \ddot{\phi} + \dot{\phi} + \sin\phi = i + i_N(\tau) \tag{9}$$

where τ is the time normalized to the factor τ_W from equation (4). This noise current produces fluctuations of the phase ϕ and a consequent time fluctuations of the pulses, like in a clock generator. In future studies we will analyze such thermal noise influence in the circuit shown in figure 4 and the probability of error switching induced in the decision component operation, i.e. the comparator in the sigma-delta modulator.

4 – NbN RSFQ CIRCUIT FOUNDRY AT CEA-GRENOBLE

The NbN RSFQ multilayer circuit technology utilizes either externally shunted NbN/MgO/NbN or self-shunted NbN/Ta_XN/NbN junctions [10], [11], [28], [29], [30]. NbN circuits are presently fabricated in a CEA-G research dedicated Clean-Room ("PROMES"- 75 mm wafers) for researches on NbN junction barriers and on RSFQ gate components, as well as in a CEA-Leti microelectronic development platform ("PLATO"- 200 mm Si wafers) for studying lithographic scaling of NbN junctions and LSI RSFQ circuit feasibility [27].

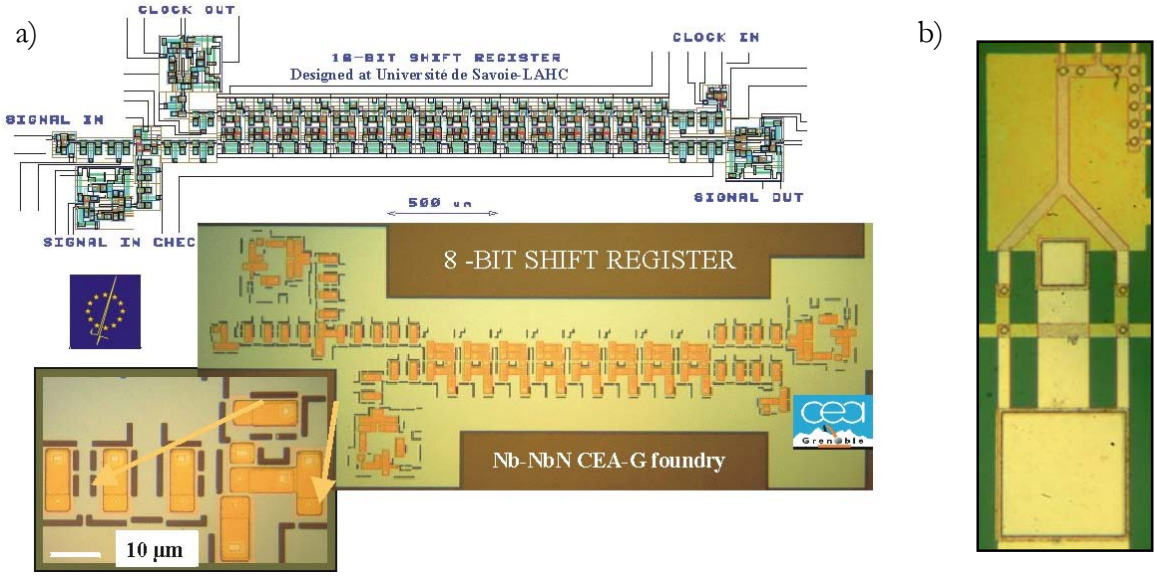

Figure 5 – Design and implementation of a) a 8 bit shift register circuit in a 3 µm diameter NbN/MgO/NbN junction technology (collaboration CEA -Grenoble/LCP- Université de Savoie/LAHC and University of Jena/IPHT through the "SCENET- Fluxonics" network [36]) and b) a clock circuit in a 3 µm NbN/Ta_XN/NbN junction technology with its test device based on a Toggle - Flip Flop.

As shown in Figure 5 and in Figure 6, existing semiconductor system design and simulation techniques has been applied to design and implement shift registers and Flip-Flop RSFQ gates. NbN as medium temperature superconductor able to operate at 10 K (because of the 16 K superconducting critical temperature of the NbN), well described by conventional "BCS" theory of superconductivity and reliable material, benefits from RSFQ libraries and foundries organized in networks such as "CONNECT" [37] for Japan or "FLUXONICS" [31] for Europe as shown in Figure 7.
Moreover, such a nitride technology (firstly based on TiN with a Tc of 4.8 K, and now based on NbN) has been recently demonstrated to be fully compatible with existing CMOS deposition, lithographic and patterning techniques, as well as large scale integration of planarized RSFQ circuits on 200 mm diameter silicon wafer at reasonable

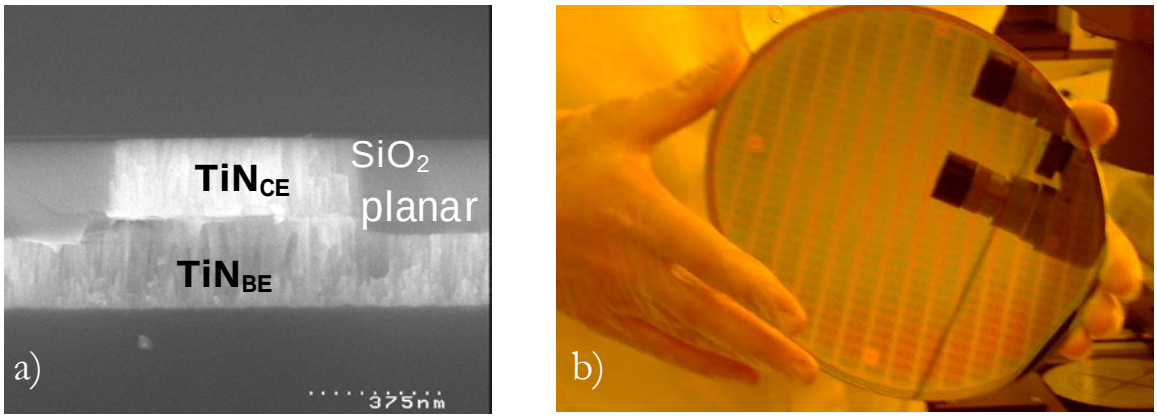

Figure 6 – Development of a 0.25 µm linewidth planarized nitride junction technology on 200 mm silicon wafers for ADC RSFQ circuits in collaboration with CEA-Leti (first demonstration on TiN junctions [27]).

fabrication cost in the CEA-Leti platform [27].

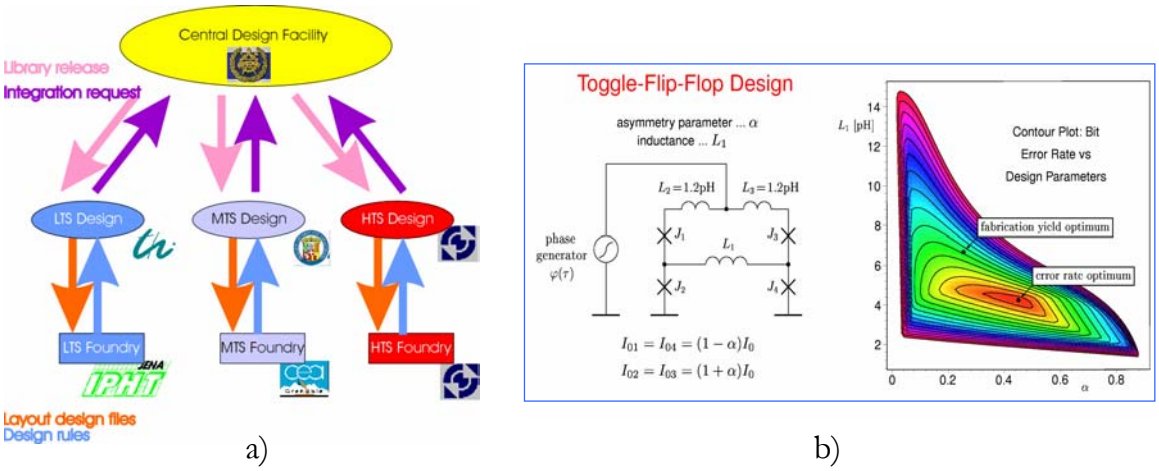

Figure 7 – a) Organization of the European RSFQ "SCENET-Fluxonics" foundry and library network [36], where NbN represents the Medium Temperature Superconductor (MTS) choice; b) Example of library based design and foundry based implementation of a T-Flip Flop with wide

By using an adapted RSFQ-"Fluxonics" library [31] and conventional packaging techniques, we present how NbN RSFQ should make feasible digital module operation for space telecom at about 100 GHz clock frequency and 10 K, temperature compatible with recently developed compact cryo-coolers [32].

The applicability of high frequency, high accuracy, and ultra-low dissipation NbN RSFQ digital functions is very promising in the next decade. Figure 8 shows the comparison of existing advanced semiconductor ADCs and forecast components including Nb and NbN RSFQ ADCs demonstration with relaxed lithographic sizes in comparison to semiconductor. Space Telecoms will finally be possible due to the development of reliable, low electrical power consuming, space qualified cryo-coolers operating at about 10K.

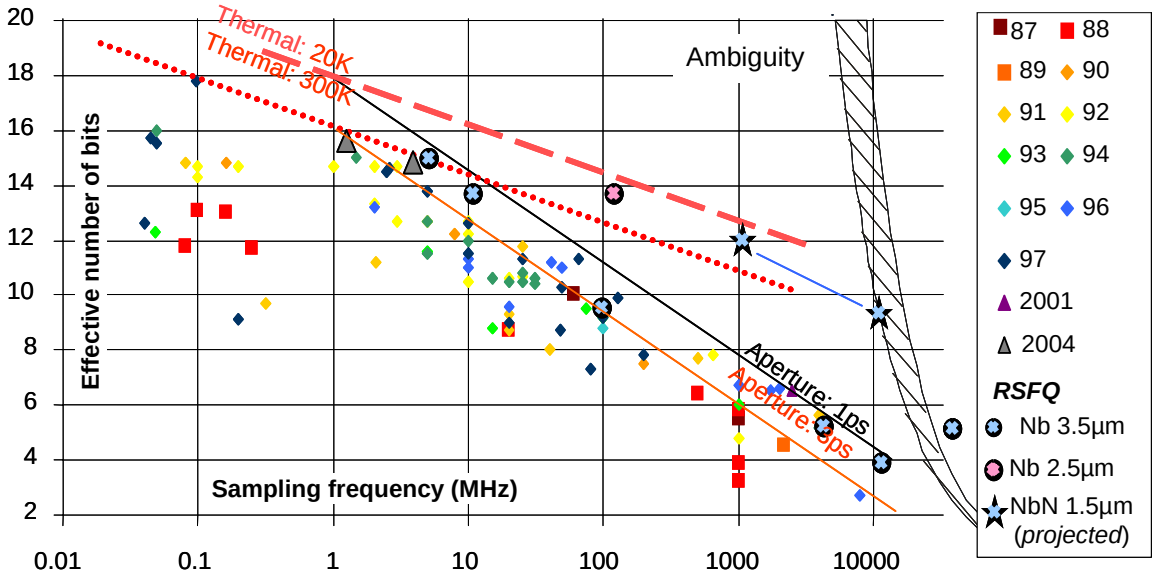

Figure 8 – Comparison of ADC technologies: semiconductor data are taken from Walden [38], complementary more recent semiconductor data, by courtesy from D. Crété, Thales and RSFQ data from ref. [3].

6 – CONCLUSION

The all digital electronics is the most efficiency way to upgrade a telecommunication charge during the satellite life at an acceptable cost and justifying an increase in the system flexibility. A good solution to this problem will be to place a large bandwidth, high dynamic range RSFQ Analog-to-Digital Converter (ADC) and very large data flow digital processors in order to operate forecast telecom signals with a sufficient sensitivity and frequency bandwidth at the antenna output.

RSFQ logics look to be one of the best examples of disruptive technology able to solve a problem probably out of the scope of most semiconductor forecasted technologies. The example of first component demonstrations in niobium and in niobium nitride based sigma-delta RSFQ modulators operating at very high speed with very low power dissipation, well beyond what will be possible with CMOS technology in the next decades, is very convincing. For instance the NbN multilayer circuit technology with NbN/Ta_XN/NbN internally shunted Josephson junctions developed at CEA-G, scalable to large circuit integration level, is able to operate at 10 K, with a sampling clock frequency of 200 GHz and more, in a compact and long life-time close cycle space qualified refrigerator. However remaining problems have to be solved and continuous work to be done in order to operate properly in the frame of a long term CE or national program, a complete space telecom system including (superconducting) multi-beam forming antennas, ADCs, routers, packet switches, DSP.

7 - BIBLIOGRAPHY

[1] W. H. W. Tuttlebee, Software Defined Radio: Facets of a developing Technology, IEEE Personal Communications, Vol. 6, No. 2, pp. 38-44, 1999.

[2] J-C Villégier, M. Maignan, “Evaluation des applications spatiales des circuits logiques supraconducteurs” Internal Technical Reports, Alcatel Space & CEA, 2003.

[3] P. Bunyk, K. Likharev and D. Zinoviev, RSFQ Technology: Physics and devices, Int. Journal on High Speed Electronics and Systems, ed. M. Rodwell, 2001.

[4] M. Schulz, The end of the road for Silicon?, Nature, vol. 399, pp 729-730, JUNE 1999.

[5] R.A. McKee et al., Crystalline Oxides on Silicon : The First Five Monolayers, Phys. Rev. Lett. 81, 3014, 1998.

[6] K. K. Likharev, and V. K. Semenov, RSFQ logic/memory family: a new Josephson-junction technology for sub-terahertz-clock-frequency digital systems, IEEE Applied Superconductivity Vol. 1, No. 1, pp. 3-28, 1991.

[7] T. Van Duzer and C. W. Turner, Principles of Superconductive Devices and Circuits, Prentice-Hall, 1999.

[8] M. Tinkham, Introduction to superconductivity, Dover Publications, Inc., Second Edition, 2004.

[9] A. Barone and G. Paternò, Physics and Applications of the Josephson Effect, Wiley, 1982.

[10] R. Setzu, N. Hadacek, V. Larrey, G. Beaudin, J-C. Villégier, NbN Josephson and Tunnel Junctions for Space THz Observation and Signal Processing, these Proceedings, 2005.

[11] V. Larrey, J-C. Villégier, M. Salez, F. Miletto-Granozio, A. Karpov, Processing and Characterization of High Jc NbN Superconducting Tunnel Junctions for THz Analog Circuits and RSFQ, IEEE Trans on Applied Superconductivity, Vol 9, N°2, pp 3216-3219, 1999.

[12] F. Furuta, Y. Suzuki, H. Hasegawa, E. Oya, A. Fujimaki, and H. Hayakawa, High Speed Operation of RSFQ circuits up to 30 GHz, Superconducting Science and Technology, Vol. 12, pp. 786-788, 1999.

[13] W. Chen et al., Rapid Single Flux Quantum T-Flip Flop Operating up to 770 GHz, IEEE Trans. on Applied Superconductivity, Vol.9, No. 2, pp. 3212-3215, 1999.

[14] V. Kaplunenko, On-chip Oscillator for High Precision RSFQ Applications, IEEE Trans. on Applied Superconductivity, vol. 13, No. 2, pp. 575-578, 2003.

[15] D. E. Kirichenko and I. V. Vernik, High Quality On-Chip Long Annular Josephson Junction Clock Source for Digital Superconducting Electronics, IEEE 2004.

[16] O.A. Mukhanov, RSFQ 1024-bit shift register for acquisition memory, IEEE Trans. on Applied Superconductivity, vol. 3, No. 4, pp. 3102-3113, 1993.

[17] F. Futura, K. Saitoh, and K. Takagi, High-Speed operation of Demultiplexer up to 56 GHz, IEEE Trans. On Applied Superconductivity, Vol. 13, No. 2, 2003.

[18] O.A. Mukhanov, "High-resolution ADC operation up to 19.6 GHz clock frequency", Superconductor Science and Technology, Vol. 14, pp. 1065-1070, 2001.

[19] T. Hashimoto, H. Hasegawa, S. Nagasaza et al., Superconducting second-order Sigma-Delta modulators utilizing multi-flux-quantum generators, IEEE Trans. On Applied Superconductivity, Vol. 11, No. 1, pp. 554-557, 2001.

[20] A. Fujimaki, K. Nakazono, M. Onogi et al., Numerical Analysis of Superconductive Oversampling Analog-to-digital Converters, IEEE Trans. On Applied Superconductivity, Vol. 13, No. 2, pp. 492-495, 2003.

[21] A. Seyka, K. Okada, Y. Nishido, A. Fujimaki, and H. Hayakawa, Demonstration of the Multi-bit Sigma-Delta A/D Converter with the Decimation Filter, to be published in IEEE Trans. On Applied Superconductivity, June 2005.

[22] J. F. Bulzachelli, A superconducting band-pass delta-sigma modulator for direct analog-to-digital conversion of microwave radio, Ph. D. thesis, MIT, June 2003.

[23] J. F. Bulzacchelli, Hae-Seung Lee, James A. Misewich and Mark B. Ketchen, Development of superconducting bandpass delta-sigma analog-to-digital converter, Physica C: Superconductivity, Vol. 412-414, Part 2, pp. 1539-1545, 2004.

[24] F. Futura, K. Saitoh, and K. Takagi, Design of Front-End Circuit for Superconductive A/D Converter and Demonstration of Operation Up to 43 GHz, IEEE Trans. On Applied Superconductivity, Vol. 14, No. 1, pp. 40-45, 2004.

[25] Q. P. Herr, K. Gaj, A. M. Herr, N. Vukovic, C. Mancini, M. F. Bocko, and M. J. Feldman, High Speed Testing of a Four-bit RSFQ Decimation Digital Filter, IEEE Trans. On Applied Superconductivity, Vol. 7, No. 2, pp. 2975-2978, 1997.

[26] A. A. Golubov, M. Yu. Kupriyanov, E. Il'ichev, The current-phase relation in Josephson junctions, Rev. of Modern Physics, Vol. 76, pp. 411-469, 2004.

[27] N. Hadacek, Ètude de films minces et de junctions Josephson en nitrures supraconducteurs (TiN et NbN), application à la logique RSFQ, PhD Thesis, Université J. Fourier, Grenoble, 2002.

[28] J-C. Villégier et al., New developments in textured and epitaxial NbN superconducting layers for ultimate sensors and RSFQ digital circuits, J. Phys. IV France, Vol.12-Pr3, pp. 129-132, 2002.

[29] J-C. Villégier et al., NbN multilayer technology on R-plane sapphire, IEEE Trans. on Applied Superconductivity, Vol. 11, No. 1, pp. 68-71, 2001.

[30] E. Baggetta, J. C. Villegier et al., New Design and Implemention of a Fast Modulator in NbN technology, to be published in IEEE trans Applied Superconductivity, June 2005.

[31] http://www.Fluxonics.org

[32] J. Olson, T. C. Nast et al., Development of a 10 K pulse tube cryo-cooler for space applications, International Cryocooler Conference, June 2002, Cambridge MA-USA.

[33] E. S. Fang, T. V. Duzer, A Josephson Integrated Circuit Simulator (JSIM) for Superconductive Electronics Application, Ext. Abst. of 1989 International Superconductive Electronics Conference (ISEC'89), Tokyo, Japan, 1989.

[34] P. D. Bradley and S. V. Rylov, A Comparison of Two Types of Sungle Flux Quantum Comparators for a Flash ADC with 10 GHz Input Bandwidth, IEEE Trans. on Applied Superconductivity, vol. 7, No. 2, pp. 2667-2680, 1997.

[35] B. Oelze, B. Ruck, and E. Sodtke at al., Investigation of the Signal Resolution of a High-Tc Balanced Comparator, IEEE Trans. on Applied Superconductivity, vol. 7, No. 2, pp. 3450-3453, 1997.

[36] « SCENET Roadmap for Superconductor Digital Electronics », Nov. 2001, Ed. H. Rogalla et al, in Fluxonics (*www.fluxonics.com*)

[37] S. Yorozu, Y. Kameda, H. Terai, A. Fujimaki, H. Yamada, and S. Tahara, A single flux quantum standard logic cell library, Physica C 378–381, pp. 1471–1474, 2002.

[38] R.H. Walden, "Performance trends for Analog-to-Digital Converters", IEEE Communications Magazine, Vol. 37, No. 2, pp. 96-101, 1999.